CHAPTER SEVENTEEN

MOS Digital Integrated Circuits

Digital Electronics.

Introduction

There are several MOS logic families used in digital ICs: NMOS, PMOS, CMOS (Complementary) , HCMOS (High density and High speed).

MOSFET transistors can be used as active devices and as load elements also.

We will emphasize on N-MOSFET (enhancement) in this chapter

General N-MOS Inverter

A generalized NMOS is shown below. The load device , may be a resistor or another MOSFET.

$$V_{IN} = V_{GS} + I_G R_G \quad (I_G R_G = 0) \qquad V_{IN} = V_{GS}$$

$$V_{OUT} = V_{DS}$$

Since I_G is negligible $I_{DD} = I_L = I_D$

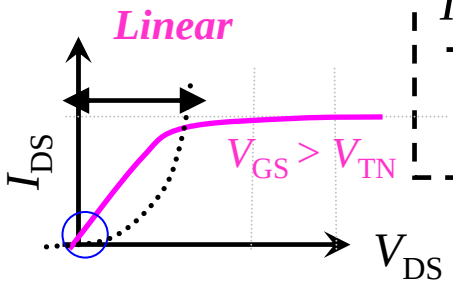
In linear mode: $(V_{GS} \geq V_{TN}), V_{DS} \leq V_{GS} - V_{TN}$

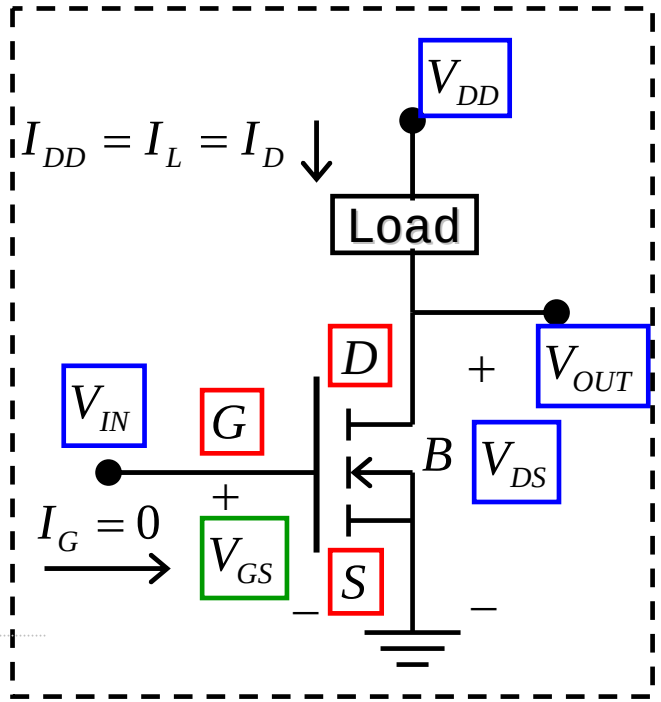
$$I_{DS} = \frac{K_n}{2}\left[2 \times (V_{GS} - V_{TN}) V_{DS} - V_{DS}^2\right]$$

In active mode: $(V_{GS} \geq V_{TN})$

$V_{DS} = 0$ Zero drain current

HOW??





Operation of N-MOS with Zero Drain Current

Graphical analysis:

If the drain current is forced to I_D~0, then the drain-to-source voltage is also forced to V_{DS}~0

Analytical analysis:

Setting I_D~0 in the linear region gives:

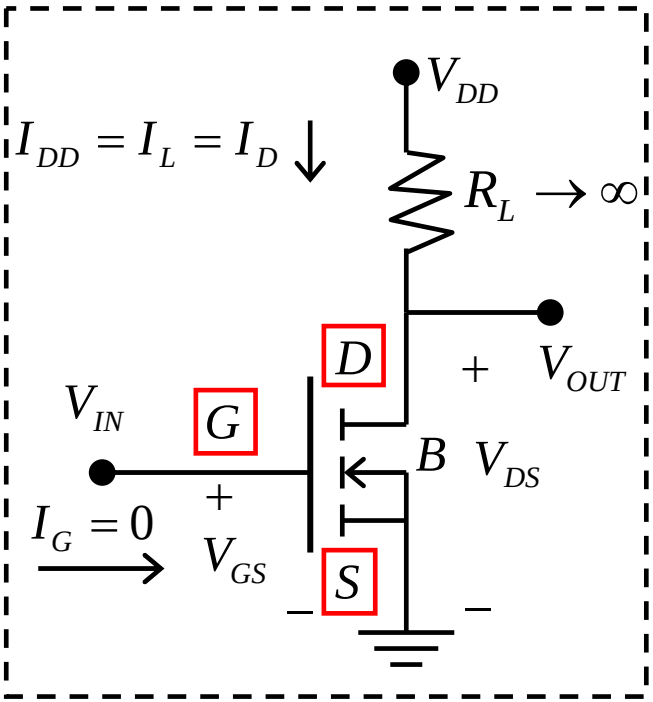
$$0 = \frac{K_n}{2}\left[2\times(V_{GS}-V_{TN})V_{DS}-V_{DS}^2\right]$$

$$V_{DS}\left[2(V_{GS}-V_{TN})-V_{DS}\right]=0$$

$$\boxed{V_{DS}=0}$$ ✓

$$V_{DS}=2(V_{GS}-V_{TN})$$ ✗

Invalid since V_{DS} has to be less than $(V_{GS}-V_{TN})$

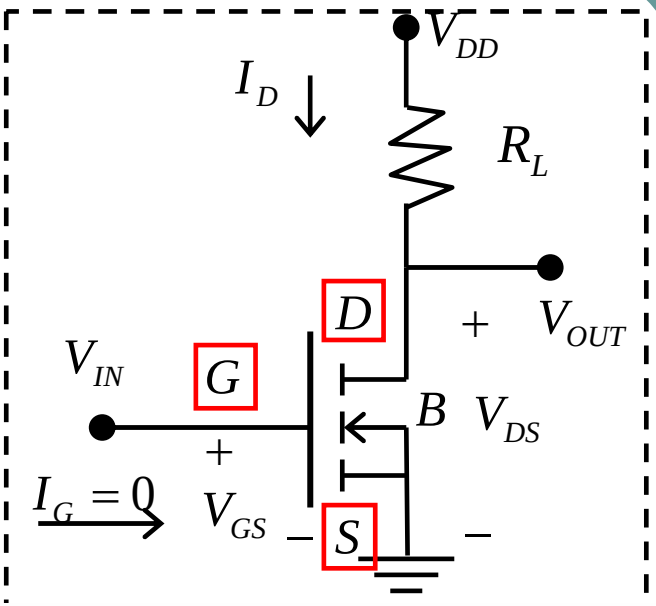


Operation of N-MOS with Zero Drain Current

Ch 17

Conclusion :

The use of N-MOS as an output pull-down device is important, i.e. with proper selection of a load device, high V_{GS} results in low V_{DS}.

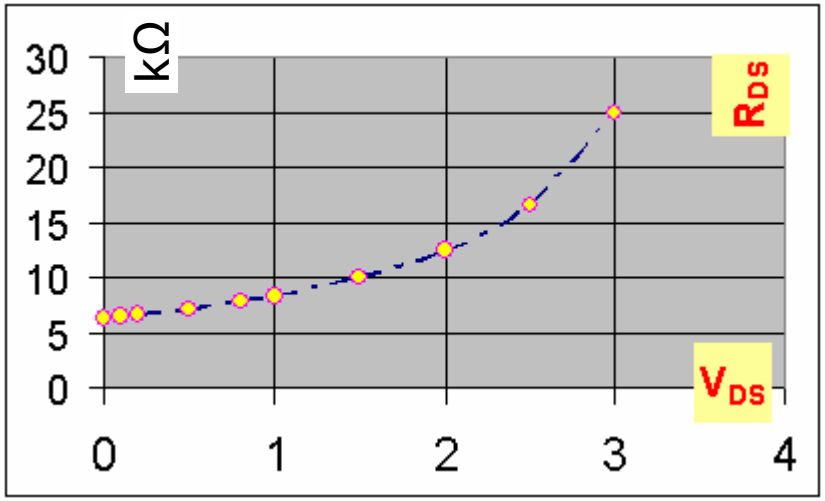


Resistance of Drain-to-Source (R_{DS}) Channel of NMOS Operating in Linear Mode (example):

Let : $V_{GS}=5V$, $V_{TN}=1V$, $K_n=40\mu A/V^2$.
Determine R_{DS}

Sol:

$$R_{DS} = \frac{1}{K_n[(V_{GS} - V_{TN}) - V_{DS}]}$$



It can be seen that the N-MOS operating in linear mode becomes more conductive as V_{DS} decreases.

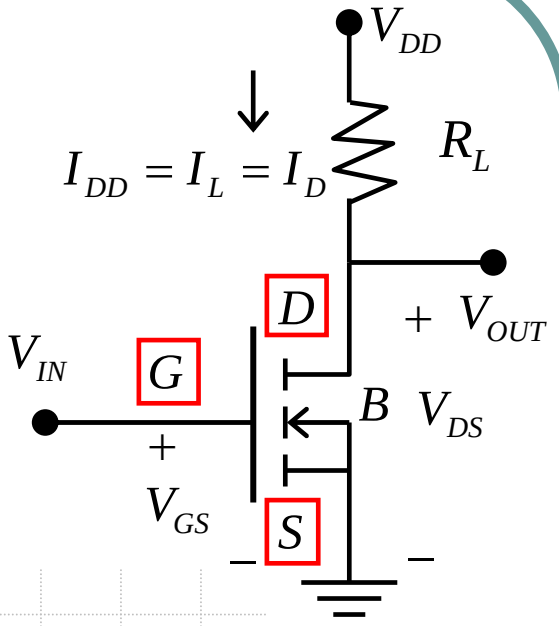
VTC of N-MOS Loaded with Resistor

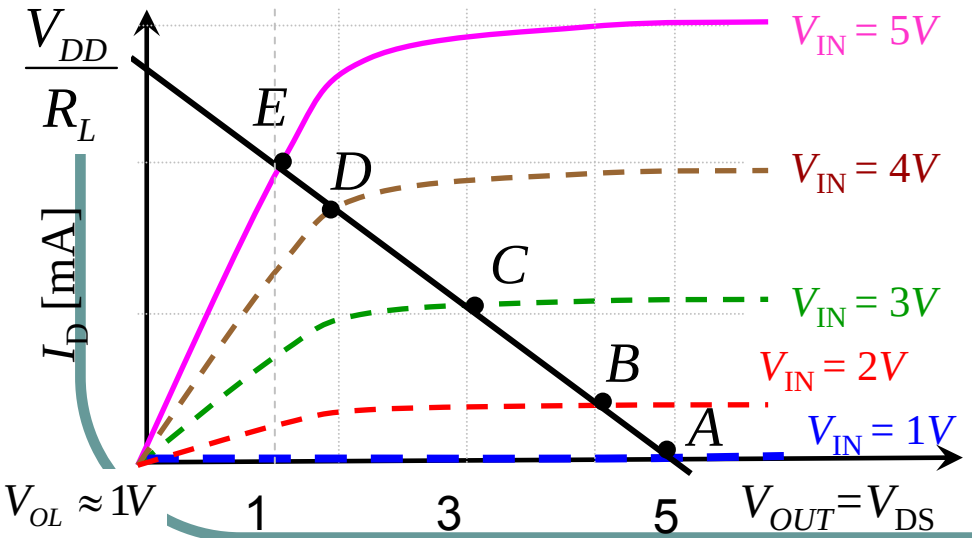
Graphical determination of VTC :

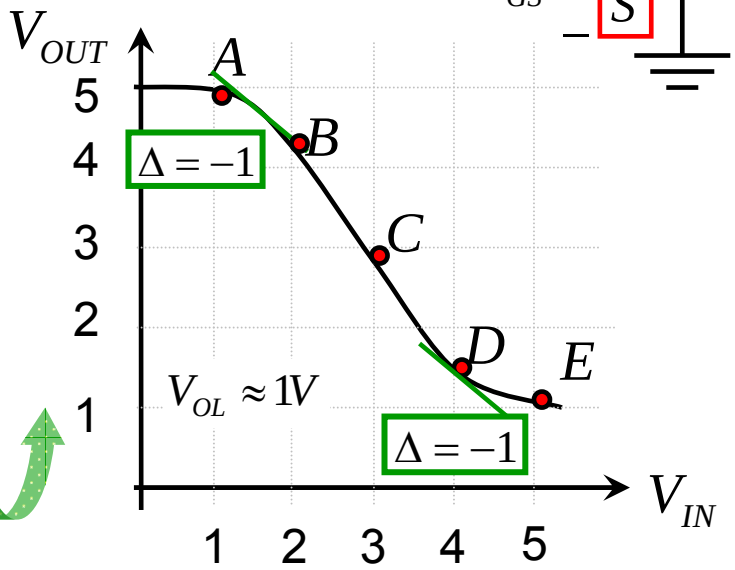
$$V_{IN} = V_{GS} \quad , \quad V_{OUT} = V_{DS}$$

Load line: $I_L = I_D = \dfrac{V_{DD} - V_{DS}}{R_L}$

From the intersections between the load line and the family of the current-voltage characteristics , the pairs of (V_{IN}, V_{OUT}) can be determined







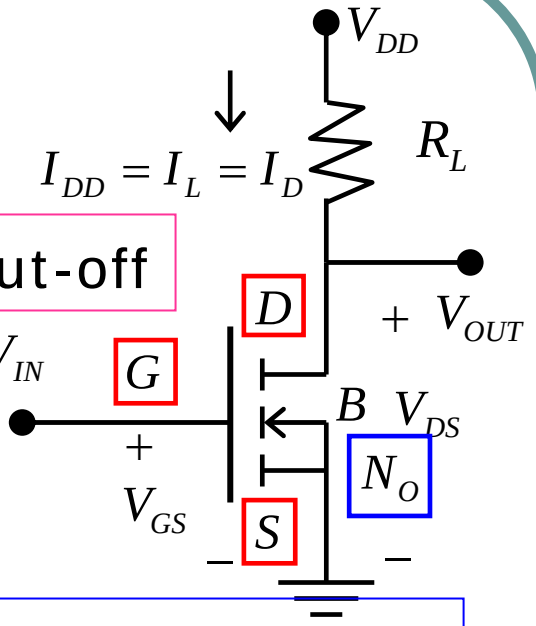
VTC of N-MOS Loaded with Resistor

Analytical determination of VTC :

V_{OH}

When V_{IN} is low, i.e. $V_{IN}=V_{GS}<V_{TN}$: → N_O is cut-off

$I_L = I_D = 0$ $\quad V_{OH} = V_{DD}$



V_{OL}

For the low output state, the N-MOS operates in linear mode:

$$I_D = \frac{K_n}{2}\left[2\times(V_{GS}-V_{TN})V_{DS}-V_{DS}^2\right]$$

Now, just as an assumption that the MOS is driven by a similar gate, i.e. $V_{IN}=V_{OH}=V_{DD}$.

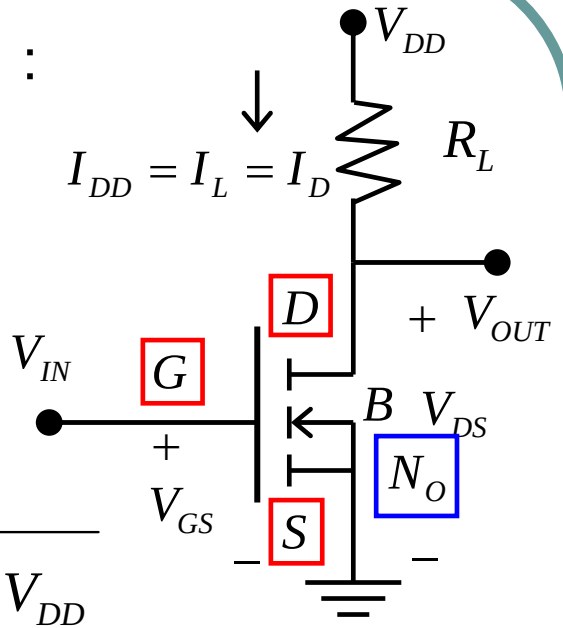
$$I_D = \frac{K_n}{2}\left[2\times(V_{DD}-V_{TN})V_{DS}-V_{DS}^2\right] = \frac{V_{DD}-V_{DS}}{R_L}$$

VTC of N-MOS Loaded with Resistor

Analytical determination of VTC :

V_{OL}

$$V_{OL}^2 - 2\left[V_{DD} - V_{TN} + \frac{1}{K_n R_L}\right]V_{OL} + \frac{2}{K_n}\frac{V_{DD}}{R_L} = 0 \quad (*)$$



$$V_{OL} = \left[V_{DD} - V_{TN} + \frac{1}{K_n R_L}\right] \pm \sqrt{\left[V_{DD} - V_{TN} + \frac{1}{K_n R_L}\right]^2 - \frac{2}{K_n}\frac{V_{DD}}{R_L}}$$

OR: neglecting V_{OL}^2 in (*)

$$V_{OL} = \frac{1}{K_n}\frac{V_{DD}}{R_L}\left[\frac{K_n R_L}{(V_{DD} - V_{TN})K_n R_L + 1}\right]$$

$$V_{OL} = \frac{V_{DD}}{(V_{DD} - V_{TN})K_n R_L + 1} = V_{DS} \le (V_{GS} - V_{TN})$$

To ensure that N_O operates in linear mode

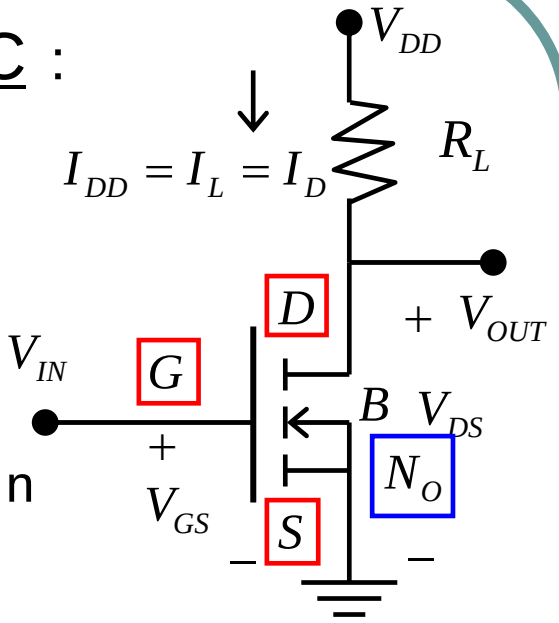
VTC of N-MOS Loaded with Resistor

Analytical determination of VTC :

V_{IL}

V_{IL} in MOSFET is defined as the input voltage slightly below $V_{OUT}=V_{OH}$ where slope=-1 or

$$\frac{dV_{OUT}}{dV_{IN}}=-1$$



For low input voltages (i.e. $V_{OUT}\rightarrow V_{OH}$), N_O is in saturation

$$I_D=\frac{K_n}{2}(V_{GS}-V_{TN})^2 \Rightarrow I_D=\frac{K_n}{2}(V_{IN}-V_{TN})^2$$

&

$$I_D=\frac{V_{DD}-V_{DS}}{R_L} \Rightarrow I_D=\frac{V_{DD}-V_{OUT}}{R_L}$$

$$\frac{dV_{OUT}}{dV_{IN}}=\frac{d}{V_{IN}}\left(V_{DD}-\frac{R_L K_n}{2}(V_{IN}-V_{TN})^2\right)=-1 \Rightarrow -R_L K_n(V_{IN}-V_{TN})=-1$$

$$V_{IN}=V_{IL}=\frac{1}{R_L K_n}+V_{TN}$$

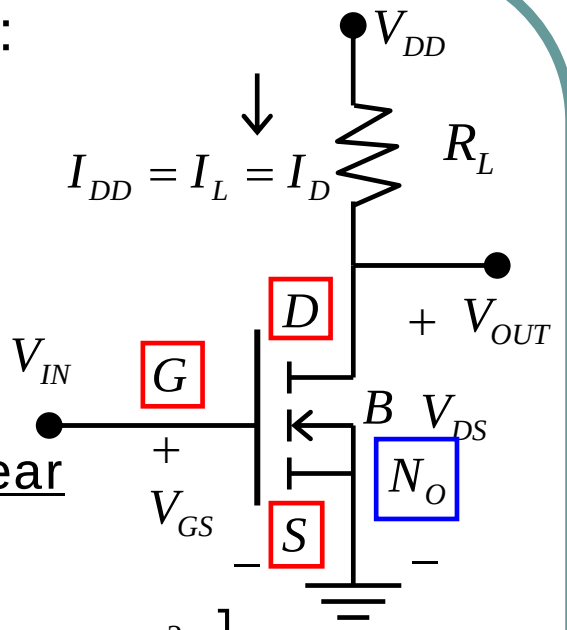
VTC of N-MOS Loaded with Resistor

Ch 17

Analytical determination of VTC :

V_{IH}

V_{IH} in MOSFET is defined as the input voltage slightly before $V_{OUT}=V_{OL}$ where slope=-1 or $\frac{dV_{OUT}}{dV_{IN}}=-1$



For high input voltages (i.e. $V_{OUT}\rightarrow V_{OL}$), N_O is in linear operation

$$I_D=\frac{K_n}{2}\left[2\times(V_{GS}-V_{TN})V_{DS}-V_{DS}^2\right]\Rightarrow I_D=\frac{K_n}{2}\left[2\times(V_{IN}-V_{TN})V_{OUT}-V_{OUT}^2\right]$$

$$\&\quad I_D=\frac{V_{DD}-V_{DS}}{R_L}\Rightarrow I_D=\frac{V_{DD}-V_{OUT}}{R_L}$$

$$V_{OUT}(IH)=\frac{V_{IH}-V_{TN}}{2}+\frac{1}{2R_LK_n}$$

$$V_{IH}-V_{TN}=\frac{\frac{-1}{2R_L}\pm\sqrt{\left(\frac{1}{2R_L}\right)^2+\frac{3}{2}\frac{V_{DD}}{R_L}K_n}}{\frac{3}{4}K_n}$$

must $V_{DS}\le(V_{GS}-V_{TN})$ i.e. $V_{OUT}(IH)\le(V_{IH}-V_{TN})$

VTC of N-MOS Loaded with Resistor

Analytical determination of VTC :

V_M Mid point

$$V_{OUT} = V_{IN} = V_M$$

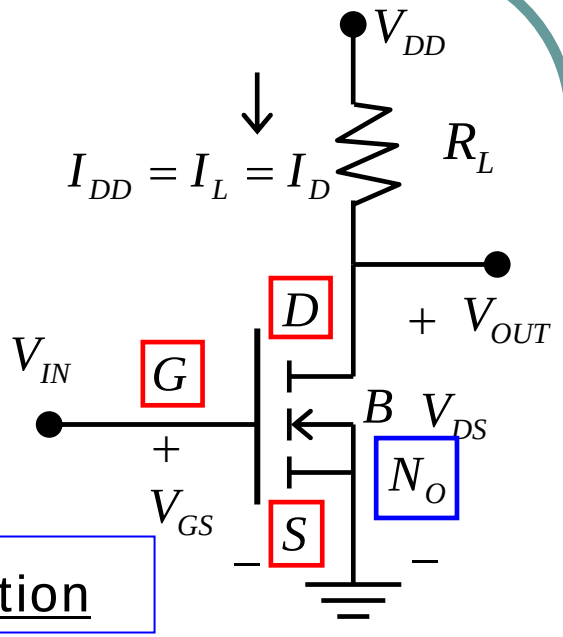
$$\Rightarrow \quad V_{DS} = V_{OUT} = V_M \quad \& \quad V_{GS} = V_{IN} = V_M$$

$$V_{DS}(sat) = V_{GS} - V_{TN}$$

$$= V_{DS} - V_{TN}$$

$$V_{DS}(sat) < V_{DS}$$

N_O is in saturation operation



$$I_D = \frac{K_n}{2}(V_M - V_{TN})^2 \quad \& \quad I_D = \frac{V_{DD} - V_M}{R_L}$$

$$\frac{K_n}{2}(V_M^2 - 2V_M V_{TN} + V_{TN}^2) = \frac{V_{DD}}{R_L} - \frac{V_M}{R_L}$$

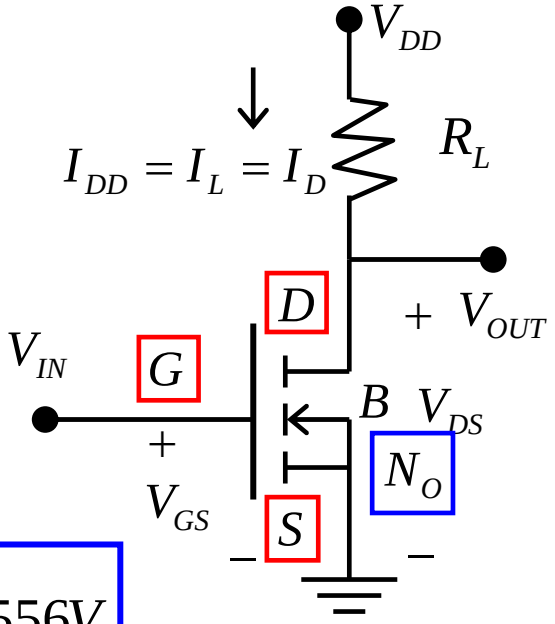
Then solve for V_M

VTC of N-MOS Loaded with Resistor

- Example

Calculate the critical values of the VTC of a resistor loaded NMOS inverter shown previously assuming:

$V_{DD}=5V$, $V_T=1$ V, $k_n=40\mu A/V^2$, $R_L=50k\Omega$,



- Solution

$$V_{OH}=V_{DD}=5V$$

$$V_{OL}=\frac{V_{DD}}{(V_{DD}-V_{TN})K_nR_L+1}=\frac{5}{(5-1)40\times10^{-3}\times50+1}=0.5556V$$

$$0556\le(5-1)ok!$$

Slide 8

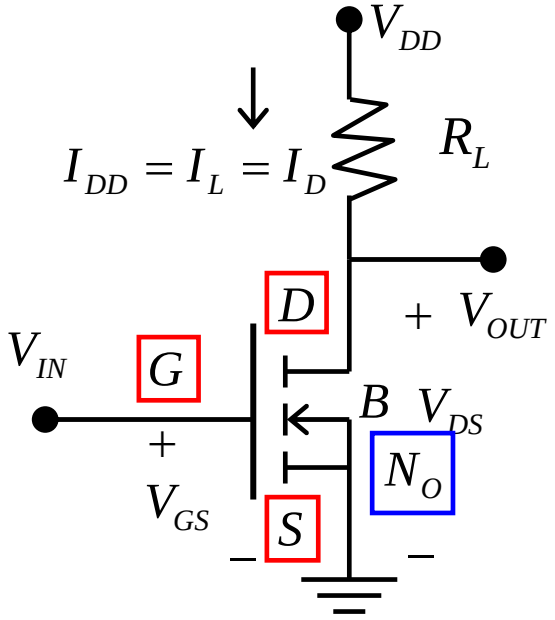
$$V_{IL}=\frac{1}{R_LK_n}+V_{TN}=\frac{1}{50\times40\times10^{-3}}+1=1.5V$$

VTC of N-MOS Loaded with Resistor

- Example

Calculate the critical values of the VTC of a resistor loaded NMOS inverter shown previously assuming:

$V_{DD}=5V$, $V_T=1$ V, $k_n=40\mu A/V^2$, $R_L=50k\Omega$,



- Solution

$$V_{IH}-V_{TN}=\frac{\frac{-1}{2R_L}\pm\sqrt{\left(\frac{1}{2R_L}\right)^2+\frac{3}{2}\frac{V_{DD}}{R_L}K_n}}{\frac{3}{4}K_n}$$

$$V_{IH}-V_{TN}=2.27 \quad \text{or} \quad -2.94$$

$$V_{IH}=3.27\,\text{V}$$

$$V_{OUT}(IH)=\frac{V_{IH}-V_{TN}}{2}+\frac{1}{2R_LK_n}=\frac{2.27}{2}+\frac{1}{4}=1.39V$$

must $V_{DS}\le(V_{GS}-V_{TN})$ *ok!*

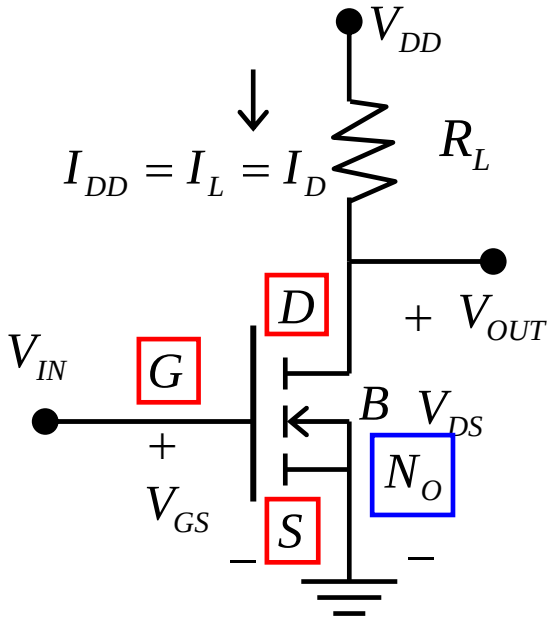
Slide 10

VTC of N-MOS Loaded with Resistor

- Example

Calculate the critical values of the VTC of a resistor loaded NMOS inverter shown, assuming:

$V_{DD}=5V$, $V_T=1$ V, $k_n=40\mu A/V^2$, $R_L=50k\Omega$,



- Solution

Solve for V_M

$$\frac{K_n}{2}\left(V_M^2-2V_MV_{TN}+V_{TN}^2\right)=\frac{V_{DD}}{R_L}-\frac{V_M}{R_L}$$

$$V_M=2.56V$$